



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,814	02/27/2002	Joseph Francis Mann	01AB162	6548

7590 03/07/2005

Ms. Susan M. Donahue  
Rockwell Automation, 704-P  
1202 South Second Street  
Milwaukee, WI 53204

EXAMINER

PERVEEN, REHANA

ART UNIT	PAPER NUMBER
----------	--------------

2116

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/083,814

**Applicant(s)**

MANN ET AL.

**Examiner**

Rehana Perveen

**Art Unit**

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,6,7,9-15,17 and 19-21 is/are rejected.
- 7) ☒ Claim(s) 5,8,16 and 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Response to Amendment***

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6, 7,9-15, 17, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission of Prior Art (AAPA), in view of Fullam et al, Patent No. 5,802,550.

As to claims 1 and 12, AAPA teaches an integrated processor system having a processing unit for performing arithmetic and logical operations (AAPA, Page 2, 0007) and a non-volatile boot memory holding a bootstrap program (AAPA, Page 2, 0007).

However, AAPA does not teach at least one internal system storage structure selected from the group consisting of caches, buffers, and registers, and the processing unit executing at least a portion of the bootstrap program using the internal system storage structure for temporary storage without access to external memory.

Fullam et al teach a processor system having at least one internal system storage structure (parameter memory) selected from a group consisting of caches,

buffers, and registers, and the processing system executing at least a portion of a bootstrap program using the internal system storage structure for temporary storage without access to an external memory (col. 1 line 65 – col. 2 line 32 and col. 6 line 39 – col. 7 line 10).

It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of AAPA and Fullam et al because both are commonly directed to processor with versatile external memory interface systems, and Fullam et al's internal storage for storing the external memory setup data, when incorporated into teachings of the AAPA, would have enabled increased flexibility by allowing the processing unit to interact with a number of different external memory types (Fullam et al, col. 1 line 65 – col. 2 line 32).

As to claims 2 and 13, AAPA teaches the system further including interface circuits for communicating electrical signals with non-memory external devices (AAPA, Page 2, 0005).

As to claims 3 and 14, Fullam et al teach a memory interface for communicating with the external memory (controller 56, figure 3). Fullam et al also teach the processing unit executes at least a portion of a bootstrap program to provide for acquisition of external memory setup data (parameters) required for the memory interface to initiate communication with an external memory (col. 6 line 39 – col. 7 line 10 and col. 7 lines 31-50).

As to claims 4 and 15, AAPA teaches the processing unit includes a network interface (AAPA, Page 2, 0005). Fullam et al teach acquisition of the external memory setup data is done through a network connection (col. 6 line 39 – col. 7 line 10 and col. 7 lines 41-50).

As to claim 6, Fullam et al teach the external non-volatile memory is a flash memory (col. 7 lines 41-42).

As to claims 7 and 17, Fullam et al teach the processing unit includes an address translation table mapping processing unit addresses to addresses of the external memory and make a temporary address translation table in a buffer memory so as to make the cache memory available for temporary storage (col. 6 line 39 – col. 7 line 10).

As to claims 9 and 19, Fullam et al teach the processing unit stores the memory setup data in the memory interface and loads additional programs for execution into external memory (figure 3).

As to claims 10 and 20, Fullam et al teach the processing unit executes at least a portion of the bootstrap program to store the memory setup data in the memory interface and executes a program contained in the external memory (col. 7 line 38 – col. 8 line 19).

As to claims 11 and 21, Fullam et al teach the memory set-up data is selected from the group consisting of the memory type, memory speed, memory size, memory parity, and memory timing (col. 7 lines 11-26 and col. 9 lines 5-7).


***Allowable Subject Matter***

Claims 5, 8, 16, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rehana Perveen whose telephone number is 571-272-3676. The examiner can normally be reached on Monday - Thursday 8:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Rehana Perveen  
Primary Patent Examiner  
Technology Center 2100